

In re Patent Application of:
PAU ET AL.
Serial No. 09/712,509
Filing Date: November 14, 2000

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The arguments supporting patentability of the claims are provided in detail below.

I. The Claims Are Patentable

Independent Claims 10, 17, 23 and 31 have been rejected over the Kadono patent in view of the Adolph et al. patent. The present invention, as recited in independent Claim 10, for example, is directed to method of producing an output bitstream of coded digital video data having a desired bit-rate different from a bit-rate of an input bitstream of coded digital video data.

The method comprises dividing the input bitstream into a sequence of coded data and into a sequence of control bits, and modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits. The method further comprises decoding the sequence of coded data for producing an intermediate sequence of data, and quantizing with a pre-established step and coding the intermediate sequence of data for producing an output sequence of coded data. The output sequence of control bits and the output sequence of coded data are merged for producing the output bitstream of coded digital video data having the desired bit-rate.

The Examiner cited the Kadono patent as disclosing a method of producing an output bitstream of coded digital video data having a desired bit-rate different from a bit-rate of an input bitstream of coded digital video data as in the claimed

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invention. As correctly noted by the Examiner, Kadono fails to disclose the output sequence of control bits and the output sequence of coded data being merged for producing an output bitstream of coded digital video data having a desired bit-rate. The Examiner cited the Adolph et al. patent to supply this noted deficiency of the Kadono patent.

The Applicants respectfully submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced. First, Kadono fails to disclose dividing the input bitstream into a sequence of coded data and into a sequence of control bits. Reference is directed to FIG. 1 and to column 18, lines 47-57 of Kadono, which provides:

"The transcoding system 10 according to this first embodiment comprises a decoding unit Da1 and an encoding unit Ea1 which has been obtained by subjecting image data to a coding process including a quantization process (first quantization process), and subjects the coded data Eg1 to a decoding process including an inverse quantization process, thereby generating decoded data Rg1. The encoding unit Ea1 subjects the decoded data Rg1 to a coding process (transcoding process) including a re-quantization process (second quantization process), thereby generating transcoded data Eg2." (Emphasis added.)

The Examiner's response is that since the quantization process does not represent coded image data, it reads on the coded control data. The Applicants' contend that the Examiner's response appears to be in contradiction to the above referenced text from Kadono. FIG. 1 in Kadono

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illustrates a decoding unit **Da1** and an encoding unit **Ea1** connected together, wherein the decoding unit receives coded data **Eg1**. Such a configuration is disclosed on page 7 of the Applicants' specification. The above text states that image data is subjected to a coding process including a quantization process, and the coded data **Eg1** is subjected to a decoding process, thereby generating decoded data **Rg1**. Consequently, since the quantization process is performed on the image data - which is subjected to a coding process - the quantization process does appear to represent coded image data. Otherwise, where is it shown that the input bit stream is divided into a sequence of coded data and into a sequence of control bits?

The Applicants thus submit that Kadono fails to disclose dividing the coded data **Eg1** (i.e., input bitstream) into a sequence of coded data and into a sequence of control bits. Instead, the coded data **Eg1** is decoded into decoded data **Rg1** for the encoding unit **Ea1**, and the coded data is also subjected to a quantization step **Qs1** for the encoding unit **Ea1** as also illustrated in FIG. 1 and as disclosed in column 18, line 58 to column 19, line 6 of Kadono.

Assuming that Kadono fails to disclose dividing the coded data **Eg1** (i.e., input bitstream) into a sequence of coded data and into a sequence of control bits, then there would be no need to merge the output sequence of control bits and the output sequence of coded data for producing the output bitstream of coded digital video data having the desired bitrate, as in the claimed invention. As noted above by the Examiner - Kadono fails to disclose the merging of the output sequence of control bits and the output sequence of coded data.

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The Applicants respectfully submit that since Kadono fails to disclose 1) dividing the coded data **Eg1** (i.e., input bitstream) into a sequence of coded data and into a sequence of control bits, and 2) merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream - then there is no motivation to modify Kadono as suggested by the Examiner in an attempt to produce the claimed invention. In fact, such a combination would produce an inoperable combination.

Moreover, Adolph et al. fails to modify the "control bits" (i.e., the system data **SYD**) as a function of the desired bit-rate of the secondary bitstream **SBS** as in the claimed invention. In Adolph et al., a primary bitstream **PBS** is converted into a secondary bitstream **SBS** with a different data rate, as best illustrated in FIG. 1. The primary bitstream **PBS** is separated by a demultiplexer **DMX** into system data **SYD**, audio data **AUD** and video data **VID**. The system data **SYD** and the audio data **AUD** are each processed by a respective processor. However, Adolph et al. fails to modify the "control bits" (i.e., the system data **SYD**) as a function of the desired bit-rate of the secondary bitstream **SBS** as in the claimed invention. The Applicants thus submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced.

Accordingly, it is submitted that independent Claim 10 is patentable over Kadono in view of Adolph et al. Independent Claims 17, 23 and 31 are similar to independent Claim 10. Therefore, it is submitted that these claims are also patentable over Kadono in view of Adolph et al. In view of the patentability of the independent claims, it is

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submitted that their dependent claims, which recite yet further distinguishing features of the invention, are also patentable. These dependent claims require no further discussion herein.

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CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 17 day of June, 2004.

Michael W. Taylor